Analysis and design of an integrated universal capacitive sensor interface

A. Heidary and G.C.M. Meijer

Electronic Instrumentation Laboratory, Delft University of Technology
Mekelweg 4, 2628 CD Delft, The Netherlands
Phone +31 15 278 5026; Fax: +31 15 278 5755; E-mail: a.heidary@tudelft.nl

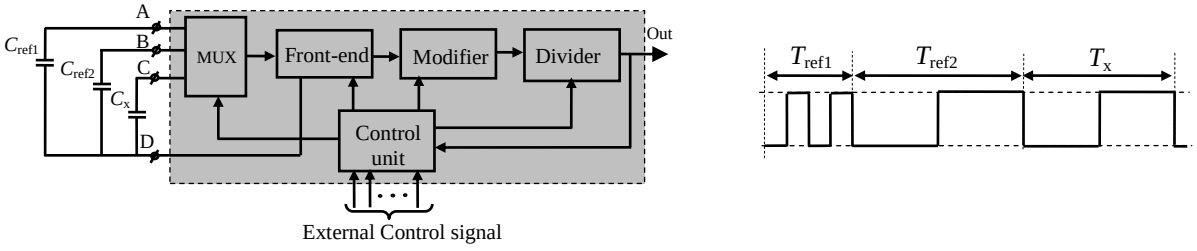
Abstract

This paper presents the most important features of an integrated universal capacitive sensor interface. The interface consists of different front-ends for floating and grounded capacitor. It has also an option for leakage-immune measurement of a floating capacitor. The interface has been optimized for different ranges of sensor capacitances from 1 pF to 1 nF. The measurement time can be set by the user from 0.1ms to 45 ms. In a certain mode for grounded capacitors, a connection cable length of up to 30 meter can be handled. The interface chip is designed in 0.7μm standard CMOS technology. The measurement result of the modes for grounded capacitors and the leakage-immunity which will be presented.

Keywords: Capacitive sensor, integrated interface, universal interface, smart sensor systems

1. Introduction

Capacitive sensor elements can be applied in many applications to measure signals such as, displacement, proximity, humidity, acceleration, liquid level, gas concentration and so on [1]. Depending on the application, the capacitive sensor can be floating (i.e. sensors in which neither of the electrodes is grounded) or grounded (i.e. sensors in which one of the electrodes is grounded) [2]. They can show a pure capacitive behavior or have resistive leakage [3]. Their values can be in a wide range from less than one pF up to hundreds of pF. Sometimes, their values can change very fast, such as in dynamic displacement measurements in a servo system, or on the other hand, their values can be semi-static, such as in capacitive liquid-level measurement systems. Besides the aforementioned sensor conditions, also the parasitic capacitances of the connecting wires should be taken into account. This paper describes a flexible universal interface, which can be used for different applications. Figure 1(a) shows a block diagram of this interface, which has been designed to be compatible with Smartec's UTI [4, 5, 12]. The interface output signal is shown in Fig. 1(b). According to the three-signal auto-calibration technique [5], a single measurement cycle consists of three phases: two for



(a) (b)

Fig. 1. (a) The main structure of interface for floating capacitor and (b) the interface output signal.

the measurement of reference capacitors C_{ref1}, C_{ref2} and a third one for the sensor capacitor C_x. The different time intervals T_{ref1}, T_{ref2} and T_x, correspond to the output signals during measuring C_{ref1}, C_{ref2} and C_x, respectively. The different periods of the output signal, can be read with a micro-controller. For identification purposes, the time interval T_{ref1} is split into two short periods [4, 5]. Data can be read via a serial port (RS232) and can be analyzed, for instance, with a Labview program.

2. The front-ends

Figure 2(a) shows the Capacitance-to-Voltage Converter (CVC), for floating capacitors [4, 5]. For the excitation and noise voltages at the input, this front-end is a normal inverting amplifier. Figure 2(b) shows some important signals. In order not to lose any charge, before transitions in the drive voltage V_{drive}, S_1 is opened. In this CVC the drive voltage has two levels of 0 V and V_{dd}. During phase 1, S_1 is closed and the drive voltage is sampled on C_x. In phase 2 the charge C_xV_{dd} is pumped in C_f which results in a jump $V_x = C_xV_{dd} / C_f$ at the output. During phase 2, the DC voltage across C_x is $V_{dd}/2$. In case of a resistive leakage of C_x, this voltage will cause a leakage current, which will result in a measurement error.

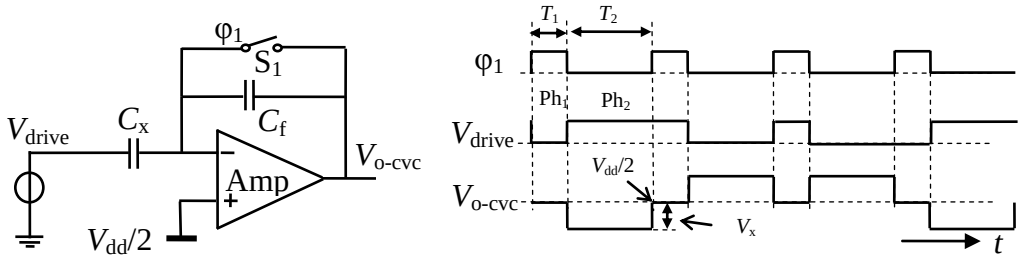


Fig. 2. (a) The CVC for high quality floating capacitor and (b) the related signal.

It is possible to modify the drive voltage in such a way, that during the charge transfer phase Ph2, the DC voltage across the sensor capacitance are at zero level. This measure will, make the circuit immune for leakage [6, 7]. Figure 3 shows the required drive voltage for leaky capacitors. Only at the transition moment, we have some DC voltage across the sensor capacitor that can cause some charge loss due to leakage.

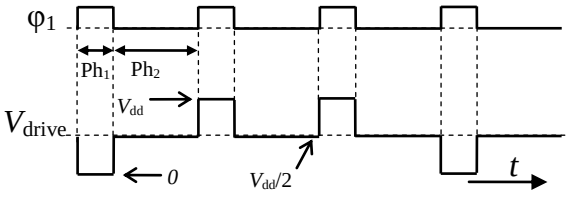


Fig. 3. The modified drive voltage for leaky capacitor, and clock signal φ_1 for the circuit of Fig. 2(a).

In this case the sampled voltage on C_x, instead of V_{dd}, is reduced to $V_{dd}/2$. Therefore, when the noise of the interface is dominated by that of the CVC (which should be the case for a good design), the useful signal is reduced with a factor of two. Therefore, we will apply this solution in the special modes for leaky capacitors only, and not in the other modes.

Due to shielding of connection cables, the sensor capacitor is accompanied by parasitic capacitances to ground (Fig. 4).

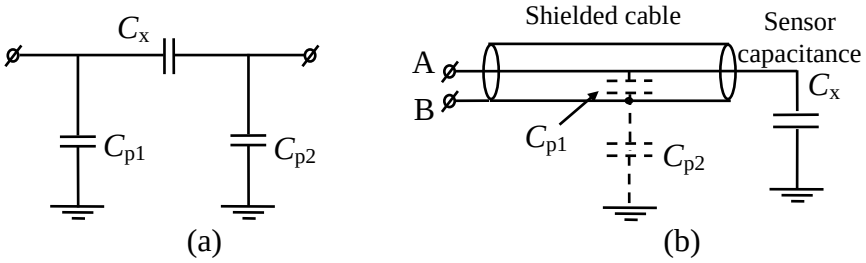


Fig. 4. The sensor capacitance with parasitics for (a) floating sensor capacitors and (b) grounded ones.

In order to measure a floating capacitor C_x independent of the parasitic capacitances, C_{p1} and C_{p2}, the sensor can be driven by a low-ohmic voltage source and the sensor current measured by a low-ohmic current meter, according to the so-called two-port measurement method, [1]. For grounded capacitors, the effect of these parasitics is reduced by using active guarding [1, 8]. In this method, using a buffer amplifier, the voltage at the cable core (point A) is feed back to the shield. When the core has a well-known voltage, instead of negative feedback, feedforward can be applied [9, 10] (Fig. 5(a)).

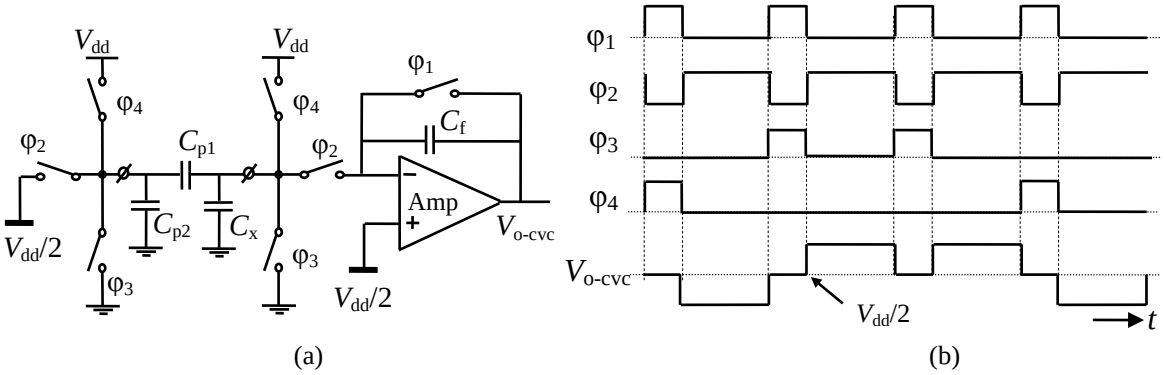


Fig. 5. (a) The Capacitance-to-Voltage-Converter for grounded capacitive sensor with feedforward elimination of the effects of parasitic capacitors; (b) some related signals.

3. Capacitance range

By looking at the front-ends (Fig. 2 and Fig. 5), it is clear that the range of the input capacitance can be changed by changing the value of the feedback capacitor C_f. Then, the next stage, being a voltage-to-period converter, can be optimized independent of the input-capacitance range. The use of an off-chip capacitor is usually avoided, but in this case it has distinctive advantages:

1. From Fig. 2 and Fig. 5, it is clear that, the value of C_f should be larger than twice as C_x. In case of rail-to-rail amplifier, $C_f = 2C_x$. Then, for large sensor capacitors, C_f be too big to be built on-chip. Whether we have to use off-chip capacitor or decrease the drive voltage, which itself decreases the signal to noise ratio and therefore decreases the resolution.
2. In case of an on-chip capacitor C_f, extra pins are needed to select a discrete capacitance range. First of all this also is not user friendly and more important than that, we can only select some discrete range which means that for specific application we may not use the whole dynamic rang. However in case of an off-chip capacitor, C_f can be select based on $C_{x\text{-}max}$ and then the whole dynamic range is used.

4. Oscillator frequency

Increasing the frequency decreases the measurement time. Moreover, when the chopper frequency is the same as the modulator frequency, a higher frequency will result in a better suppression of low-frequency noise and interference.

In switched-capacitor circuits, the maximum frequency will be limited by the required accuracy [11]. Due to parasitic capacitances, the CVC will limit the upper-limit of the frequency. Since the charge transfer time constant is different for different parasitic capacitances, in case of a single frequency as is used in the UTI [12], the worst case should be considered. However if we use different frequency which can be set by the user, then in case of small parasitic, measurement can be done faster. Changing frequency is implemented with changing the integrator current I_{int}, [4, 5].

5. Measurement result for grounded and leaky capacitor interface

For test purposes, the interfaces for grounded and leaky capacitive sensors have seperately been designed and implemented, using 0.7 μm standard CMOS technology. In each case, the interface consumes about 1 mA, and the supply voltage is 5 V.

The main objective of the interface for leaky capacitors was to measure a sensor capacitance independent of its leakage. Figure 6 shows the simulated and measured relative error $(C_x - C_{x0})/C_{x0}$ versus the leakage conductance, for C_x=220 pF [7].

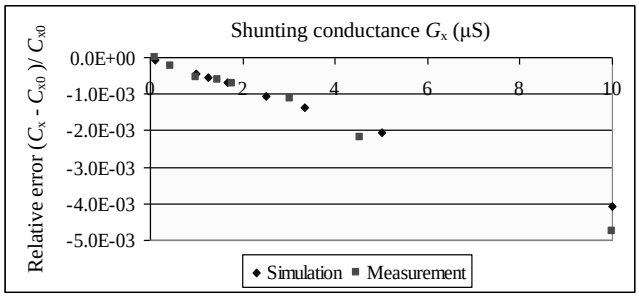


Fig. 6. The relative error in the leaky capacitor-mode versus the shunting conductance for C_x = 220pF.

For the interface for grounded capacitive sensor, the main objective was to measure a sensor capacitance C_x, while being immune for cable capacitance. Figure 7 shows the measured error versus the input capacitance C_x for four cable lengths [10].

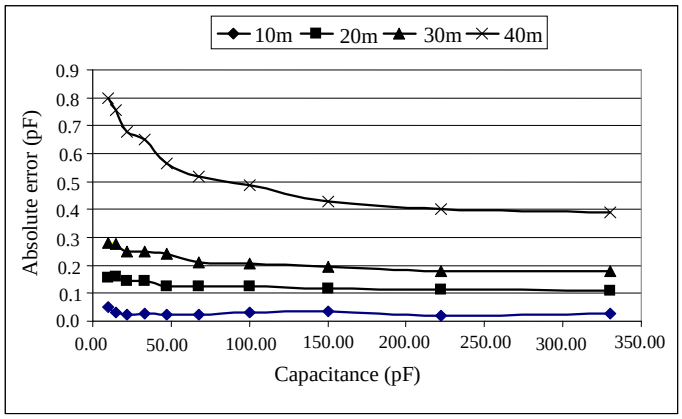


Fig. 7. Measured error in the grounded-capacitor mode versus C_x for four different cable lengths.

6. Conclusion

An integrated universal capacitive sensor interface has been proposed. Different requirements such as capacitance range, measurement speed, and the circuit implementation have discussed. Although the final interface is not yet completed, two primary interfaces, for grounded capacitive sensors and for leakage-immune measurements have been designed and implemented in 0.7 μm standard CMOS technology. The measurement results for the interface for leaky capacitors show that, when measuring a 220 pF capacitance, the relative error caused by a leakage resistor of 220 kΩ is less than 0.2%. The measurement results for the interface for grounded capacitive sensor show that the use of long connection cable, with a length up to 30 meter, will cause an absolute error of less than 0.3pF for a sensor capacitor in the range of 10 pF to 330 pF.

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